

The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (presently amended) A method of filling gaps on a semiconductor substrate, the method comprising:
  - (a) partially filling a gap on a semiconductor substrate with a dielectric using a high density plasma chemical vapor deposition process and deposition chemistry comprising a silicon-containing dielectric precursor;
  - (b) partially removing dielectric deposited in the gap from the gap opening by an etch back process conducted with etch process chemistry free of silicon-containing dielectric precursor and consisting essentially of hydrogen, wherein the substrate is biased during the etch back process and the etch rate is determined by the substrate bias power;
  - (c) further filling of the partially filled gap by a high density plasma chemical vapor deposition process and deposition chemistry comprising a silicon-containing dielectric precursor.
2. (original) The method of claim 1, wherein (b) and (c) are repeated until the gap is filled.
3. (original) The method of claim 1, wherein (b) comprises a substantially isotropic plasma etch.
4. (original) The method of claim 1, wherein the etch rate increases with increasing substrate bias power.
5. (original) The method of claim 1, wherein the substrate bias power is set between 500 and 5000W.
6. (original) The method of claim 1, wherein the bias to source plasma power ratio for substrate bias power is at least 0.5.
7. (original) The method of claim 1, wherein the bias to source plasma power ratio for substrate bias power is about 0.75.
8. (original) The method of claim 1, wherein the etch process chemistry further comprises an inert gas selected from the group consisting of He, Ar and N<sub>2</sub>.

10/733,858  
NOVLP090/2888

9. (original) The method of claim 8, wherein the etch plasma chemistry further comprises He.
10. (original) The method of claim 1, wherein the deposition and etch steps are conducted in a single plasma reactor process chamber.
11. (original) The method of claim 10, wherein the plasma generated for deposition and etch is a radio frequency based inductively coupled plasma.
12. (original) The method of claim 1, wherein the etch is conducted using plasma process chemistry and reactor conditions as follows:

Wafer temp (°C)	250 – 700
H <sub>2</sub> (sccm)	300-2000
He (sccm)	50-1000
Pressure (mTorr)	0.2-100
Bias (HF RF) Power (W)	500-7000
Source (LF) Power (W)	2000-7000

13. (original) The method of claim 12, wherein the etch is conducted using plasma process chemistry and reactor condition as follows:

Wafer temp (°C)	650
H <sub>2</sub> (sccm)	800
He (sccm)	300
Pressure (mTorr)	7.0
Bias (HF RF) Power (W)	3000
Source (LF) Power (W)	4000

14. (original) The method of claim 1, wherein the deposited dielectric is silicon dioxide (SiO<sub>2</sub>).

10/733,858  
NOVLP090/2888

15. (original) The method of claim 14, wherein the deposition is conducted using process chemistry as follows:

Gas	Flow Rate (sccm)
SiH <sub>4</sub>	10-300
O <sub>2</sub>	20-1000
He	0-1000
H <sub>2</sub>	0-5000

16. (presently amended) A method of etching a dielectric on a semiconductor substrate, the method comprising:

removing dielectric on the substrate by a biased plasma etch process conducted with process chemistry free of silicon-containing dielectric precursor and consisting essentially of hydrogen.

17. (original) The method of claim 16, wherein the etching is part of a multi-step etch-enhanced gap fill process and the dielectric is partially removed from the gap opening.

18. (original) The method of claim 16, wherein the etch plasma chemistry further comprises He.

19. (original) The method of claim 18, wherein the etch is conducted using plasma process chemistry and reactor conditions as follows:

Wafer temp (°C)	250 - 700
H <sub>2</sub> (sccm)	300-2000
He (sccm)	50-1000
Pressure (mTorr)	0.2-100
Bias (HF RF) Power (W)	500-7000
Source (LF) Power (W)	2000-7000

20. (original) The method of claim 18, wherein the etch is conducted using plasma process chemistry and reactor condition as follows:

Wafer temp (°C)	650
H <sub>2</sub> (sccm)	800
He (sccm)	300
Pressure (mTorr)	7.0
Bias (HF RF) Power (W)	3000
Source (LF) Power (W)	4000